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CAMPBELL STEPHENSON LLP
11401 CENTURY OAKS TERRACE
BLDG. H, SUITE 250
AUSTIN, TX 78758

EXAMINER	
TANG, KAREN C	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/978,475	ROSE ET AL.	
	Examiner	Art Unit	
	KAREN C. TANG	2451	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10-16,24-27 and 30-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10-16,24-27 and 30-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 1-8, 10-16, 24-27, 30-38 are presented for examination.

2. Prosecution is reopened, the prior Final Rejection filed on 08/05/08 is now withdrawn due to the Pre-Appeal Conference Decision.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-8, 10-16, 24-27, 30-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kano et al hereinafter Kano (US 5,838,690) in view of Lay (US 2002/0176357) in further view of Aimoto et al (US 6,870,854),

3. Referring to Claim 1, Kano discloses a method comprising: a transmitting device transmitting data at a first rate to a memory for storage therein during a first period of time (refer to Col 5, Lines 20-27); generating a first data quantity value representing a quantity of data stored in the memory at a first point in time (refer to Col 5, Lines 9-11), comparing a data quantity value associated with the quantity of data to a first predetermined value (refer to Col 5, Lines 20-27); in response to comparing the first data quantity value to the first predetermined value, the transmitting device transmitting data at a second non-zero rate to the memory for storage therein during a second period of time (refer to Col 5, Lines 25-27); wherein the second period of time is subsequent to the first period of time (refer to Col 5, Lines 25-27), and; wherein

the second non-zero rate is greater than the first non-zero rate (max communication rate is greater than prior rate, refer to Col 5, Lines 27).

Although Kano disclosed the invention substantially as claimed, Kano did not explicitly disclosing "comparing the first data quantity value representing a quantity of data stored in the memory with a first predetermined value"

Lay, in analogous art, disclosing that "comparing the first data quantity value representing a quantity of data stored in the memory with a first predetermined value (refer to par 0010)"

It would have been obvious to one of ordinary skill in the art to combine Kano with Lay's systems because Lay's teaching of "comparing the first data quantity value representing a quantity of data stored in the memory with a first predetermined value" would improve the system processing speed and off load the host CPU so that instruction decision do not delay packet forwarding.

Although Kano and Lay disclosed the invention substantially as claimed, Kano and Lay did not explicitly disclosing that "modified the first predetermined value"

Aimoto, in analogous art, disclosing that "modified the first predetermined value (refer to Col 10, Lines 35-50)"

It would have been obvious to one of ordinary skill in the art to combine Kano and Lay with Aimoto's system because Aimoto's teaching of " modified the first predetermined value" would improve Kano and Lay's system by allow efficiently utilizing the buffer and provide better judgment for the congestion of the whole buffer in regard to the total number of cell available.

4. Referring to Claim 2. Kano, Lay and Aimoto disclosed the method of claim 1. Although Kano disclosed the invention substantially as claimed, Kano did not explicitly disclosing the buffer used in the system is a FIFO buffer.

Lay, in analogous art, disclosing that buffer used in the system is a FIFO buffer (refer to par 0029).

It would have been obvious to one of ordinary skill in the art to combine Kano with Lay's systems because Lay's teaching of "buffer used in the system is a FIFO buffer" would improve the system processing speed and off load the host CPU so that instruction decision do not delay packet forwarding.

5. Referring to Claim 3. Kano, Lay and Aimoto disclosed the method of claim. Although Kano disclosed the invention substantially as claimed, Kano did not explicitly disclosing "wherein the transmitting device is contained in a switching fabric, wherein the memory is contained in a line card coupled to the switching fabric via a data link, and wherein the transmitter transmits data via the data link to the memory for storage therein."

Lay, in analogous art, disclosing that "wherein the transmitting device is contained in a switching fabric, wherein the memory is contained in a line card coupled to the switching fabric via a data link, and wherein the transmitter transmits data via the data link to the memory for storage therein (refer to Par 0026, 0027 and 0028)"

It would have been obvious to one of ordinary skill in the art to combine Kano with Lay's systems because Lay's teaching of "wherein the transmitting device is contained in a switching fabric, wherein the memory is contained in a line card coupled to the switching fabric via a data

link, and wherein the transmitter transmits data via the data link to the memory for storage therein" would improve the system processing speed and off load the host CPU so that instruction decision do not delay packet forwarding.

6. Referring to Claim 4. Kano, Lay and Aimoto disclosed the method of claim 1 further comprising: generating a rate control signal (refer to Col 5, Lines 1-30); and transmitting the rate control signal to the transmitting device to instruct the transmitting device to stop transmitting data at the first non-zero rate and start transmitting data at the second non-zero rate (refer to Col 5, Lines 1-30); wherein the transmitting device stops transmitting data to the memory device at the first data rate and starts transmitting data to the memory device at the second data rate in response to the transmitting device receiving the rate control signal (refer to Col 5, Lines 1-30).

7. Referring to Claim 6. Kano, Lay and Aimoto disclosed the method of claim 4. Kano further disclosing comparing the first data quantity value to a plurality of predetermined values (refer to Col 5, Lines 1-30), wherein the first predetermined value is one of the plurality of first predetermined values (plurality of thresholds, refer to Col 5, Lines 1-30); wherein the rate control signal is generated in response to comparing the a data quantity value associated with the first data quantity value to the plurality of predetermined values (refer to Col 5, Lines 1-30).

Although Kano disclosed the invention substantially as claimed, Kano did not explicitly disclosing "comparing the first data quantity value representing a quantity of data stored in the memory with a first predetermined value"

Lay, in analogous art, disclosing that "comparing the first data quantity value representing a quantity of data stored in the memory with a first predetermined value (refer to par 0010)"

It would have been obvious to one of ordinary skill in the art to combine Kano with Lay's systems because Lay's teaching of "comparing the first data quantity value representing a quantity of data stored in the memory with a first predetermined value" would improve the system processing speed and off load the host CPU so that instruction decision do not delay packet forwarding.

8. Referring to Claim 7. Kano, Lay and Aimoto disclosed the method of claim 4. Kano further disclosing: generating a second data quantity value representing a quantity of data stored in the memory device at a second point in time (refer to Col 5, Lines 1-30), wherein the second point in time is prior to the first point in time (refer to Col 5, Lines 1-30); comparing a data quantity associated with the first data quantity value to the second data quantity value (refer to Col 5, Lines 1-30); wherein the rate control signal is generated if comparing a data quantity associated with the first data quantity value is not equal to the second data quantity value (refer to Col 5, Lines 1-30);

Although Kano disclosed the invention substantially as claimed, Kano did not explicitly disclosing "comparing the first data quantity value representing a quantity of data stored in the memory with a first predetermined value"

Lay, in analogous art, disclosing that "comparing the first data quantity value representing a quantity of data stored in the memory with a first predetermined value (refer to par 0010)"

It would have been obvious to one of ordinary skill in the art to combine Kano with Lay's systems because Lay's teaching of "comparing the first data quantity value representing a quantity of data stored in the memory with a first predetermined value" would improve the system processing speed and off load the host CPU so that instruction decision do not delay packet forwarding.

9. Referring to Claim 8. Kano, Lay and Aimoto disclosed the method of claim 1 wherein generating the first data quantity value comprises: generating total data input count at the first point in time, wherein the total data input count represents a quantity of data input to the memory device during a period of time ending in the first point in time (refer to Col 5, Lines 1-27); generating total data output count at the first point in time, wherein the total data output count represents a quantity of data output from the memory device during the period of time ending in the first point in time (refer to Col 5, Lines 1-27);

Although Kano and Lay disclosed the invention substantially as claimed, Kano and Lay did not explicitly disclosing that "subtracting the total data output count from total data input count"

Aimoto, in analogous art, disclosing that "subtracting the total data output count from total data input count value (refer to Cik 13m Kubes 20-35)"

It would have been obvious to one of ordinary skill in the art to combine Kano and Lay with Aimoto's system because Aimoto's teaching of " subtracting the total data output count from total data input count" would improve Kano and Lay's system by allow efficiently utilizing the buffer and provide better judgment for the congestion of the whole buffer in regard to the total number of cell available.

10. Referring to Claim 10. Kano discloses an apparatus comprising: a memory device configured to receive data from a transmitting device for storage therein (determine the size of the buffer not used by generating the count of a data used in buffer, refer to Col 5, Lines 9-11);

a first circuit configured to generate and transmit a rate control signal instructing the transmitting device to stop transmitting data to the memory device at a

first non-zero rate and to begin transmitting data to the memory device at a second non-zero rate wherein the second non-zero rate is greater than the first non-zero rate (max communication rate is greater than prior rate, refer to Col 5, Lines 5-27);

a second circuit for generating a first data quantity value representing a quantity of data stored in the memory device at a first point in time (determine the size of the buffer not used by generating the count of a data used in buffer, refer to Col 5, Lines 9-11); and

a first comparing circuit for comparing the first data quantity value to a first predetermined value, wherein the first comparing circuit generates the rate control signal in response to comparing the a data quantity associated with the first data quantity value to the first predetermined value (refer to Col 5, Lines 20-27);

Although Kano disclosed the invention substantially as claimed, Kano did not explicitly disclosing "comparing the first data quantity value representing a quantity of data stored in the memory with a first predetermined value"

Lay, in analogous art, disclosing that "comparing the first data quantity value representing a quantity of data stored in the memory with a first predetermined value (refer to par 0010)"

It would have been obvious to one of ordinary skill in the art to combine Kano with Lay's systems because Lay's teaching of "comparing the first data quantity value representing a quantity of data stored in the memory with a first predetermined value" would improve the system processing speed and off load the host CPU so that instruction decision do not delay packet forwarding.

Although Kano and Lay disclosed the invention substantially as claimed, Kano and Lay did not explicitly disclosing that "modified the first predetermined value"

Aimoto, in analogous art, disclosing that "modified the first predetermined value (refer to Col 10, Lines 35-50)"

It would have been obvious to one of ordinary skill in the art to combine Kano and Lay with Aimoto's system because Aimoto's teaching of " modified the first predetermined value" would improve Kano and Lay's system by allow efficiently utilizing the buffer and provide better judgment for the congestion of the whole buffer in regard to the total number of cell available.

11. Referring to Claim 11. Kano, Lay and Aimoto disclosed the apparatus of claim 10. Although Kano disclosed the invention substantially as claimed, Kano did not explicitly disclosing the buffer used in the system is a FIFO buffer.

Lay, in analogous art, disclosing that buffer used in the system is a FIFO buffer (refer to par 0029).

It would have been obvious to one of ordinary skill in the art to combine Kano with Lay's systems because Lay's teaching of "buffer used in the system is a FIFO buffer" would improve the system processing speed and off load the host CPU so that instruction decision do not delay packet forwarding.

12. Referring to Claim 12. Kano, Lay and Aimoto disclosed the apparatus of claim 10. Kano disclosed the invention substantially as claimed, Kano did not explicitly disclosing "wherein the transmitting device is contained in a switching fabric, wherein the memory is contained in a line card coupled to the switching fabric via a data link, and wherein the transmitter transmits data via the data link to the memory for storage therein."

Lay, in analogous art, disclosing that "wherein the transmitting device is contained in a switching fabric, wherein the memory is contained in a line card coupled to the switching fabric via a data link, and wherein the transmitter transmits data via the data link to the memory for storage therein (refer to Par 0026, 0027 and 0028)"

It would have been obvious to one of ordinary skill in the art to combine Kano with Lay's systems because Lay's teaching of "wherein the transmitting device is contained in a switching fabric, wherein the memory is contained in a line card coupled to the switching fabric via a data

link, and wherein the transmitter transmits data via the data link to the memory for storage therein" would improve the system processing speed and off load the host CPU so that instruction decision do not delay packet forwarding.

13. Referring to Claim 14. Kano, Lay and Aimoto disclosed the apparatus of claim 10 further comprising: a plurality of comparing circuits, each one of which is configured to compare the first data quantity value to a respective one of a plurality of predetermined values (refer to Col 5, Lines 1-30), wherein the first comparing circuit is one of the plurality of comparing circuits (refer to Col 5, Lines 1-30), and wherein the first predetermined value is one of the plurality of first predetermined values (refer to Col 5, Lines 1-30); wherein the circuit generates the rate control signal in response to comparing the first data quantity value to the plurality of predetermined values (refer to Col 5, Lines 1-30).

14. Referring to Claim 15. Kano, Lay and Aimoto disclosed the apparatus of claim 10. Kano further disclosing: a third circuit for generating a second data quantity value representing a quantity of data stored in the memory device at a second point in time (refer to Col 5, Lines 1-30), wherein the second point in time is prior to the first point in time (refer to Col 5, Lines 1-30); a second comparing circuit for comparing a data quantity associated with the first data quantity value to the second data quantity value (refer to Col 5, Lines 1-30); wherein the rate control signal is generated if comparing a data quantity associated with the first data quantity value is not equal to the second data quantity value (refer to Col 5, Lines 1-30);

Although Kano disclosed the invention substantially as claimed, Kano did not explicitly disclosing "comparing the first data quantity value representing a quantity of data stored in the memory with a first predetermined value"

Lay, in analogous art, disclosing that "comparing the first data quantity value representing a quantity of data stored in the memory with a first predetermined value (refer to par 0010)"

It would have been obvious to one of ordinary skill in the art to combine Kano with Lay's systems because Lay's teaching of "comparing the first data quantity value representing a quantity of data stored in the memory with a first predetermined value" would improve the system processing speed and off load the host CPU so that instruction decision do not delay packet forwarding.

15. Referring to Claim 16. Kano, Lay and Aimoto disclosed the apparatus of claim 15 wherein the first and second circuits are the same circuits (refer to Col 5, Lines 1-30).

16. Referring to Claim 24. Kano discloses an apparatus comprising: a memory device configured to receive data from a transmitting device for storage therein; a first means for generating and transmitting a rate control signal instructing the transmitting device to stop transmitting data to the memory device at a first non-zero rate and to begin transmitting data to the memory device at a second non-zero rate wherein the second non-zero rate is greater than the first non-zero rate (max communication rate is greater than prior rate, refer to Col 5, Lines 5-27), a second means for generating a first data quantity value representing a quantity of data stored in

the memory device at a first point in time (determine the size of the buffer not used by generating the count of a data used in buffer, refer to Col 5, Lines 9-11); a third means for comparing a data quantity associated with the first data quantity value to a first predetermined value (refer to Col 5, Lines 20-27); wherein the first means generates the rate control signal in response to comparing the first data quantity value to the first predetermined value (refer to Col 5, Lines 1-30).

Although Kano disclosed the invention substantially as claimed, Kano did not explicitly disclosing "comparing the first data quantity value representing a quantity of data stored in the memory with a first predetermined value"

Lay, in analogous art, disclosing that "comparing the first data quantity value representing a quantity of data stored in the memory with a first predetermined value (refer to par 0010)"

It would have been obvious to one of ordinary skill in the art to combine Kano with Lay's systems because Lay's teaching of "comparing the first data quantity value representing a quantity of data stored in the memory with a first predetermined value" would improve the system processing speed and off load the host CPU so that instruction decision do not delay packet forwarding.

Although Kano and Lay disclosed the invention substantially as claimed, Kano and Lay did not explicitly disclosing that "modified the first predetermined value"

Aimoto, in analogous art, disclosing that "modified the first predetermined value (refer to Col 10, Lines 35-50)"

It would have been obvious to one of ordinary skill in the art to combine Kano and Lay with Aimoto's system because Aimoto's teaching of " modified the first predetermined value" would improve Kano and Lay's system by allow efficiently utilizing the buffer and provide better judgment for the congestion of the whole buffer in regard to the total number of cell available.

17. Referring to Claim 25. Kano, Lay and Aimoto disclosed the apparatus of claim 24. Although Kano disclosed the invention substantially as claimed, Kano did not explicitly disclosing the buffer used in the system is a FIFO buffer.

Lay, in analogous art, disclosing that buffer used in the system is a FIFO buffer (refer to par 0029).

It would have been obvious to one of ordinary skill in the art to combine Kano with Lay's systems because Lay's teaching of "buffer used in the system is a FIFO buffer" would improve the system processing speed and off load the host CPU so that instruction decision do not delay packet forwarding.

18. Referring to Claim 26. Kano, Lay and Aimoto disclosed the apparatus of claim 24.

Kano disclosed the invention substantially as claimed, Kano did not explicitly disclosing "wherein the transmitting device is contained in a switching fabric, wherein the memory is contained in a line card coupled to the switching fabric via a data link, and wherein the transmitter transmits data via the data link to the memory for storage therein."

Lay, in analogous art, disclosing that "wherein the transmitting device is contained in a switching fabric, wherein the memory is contained in a line card coupled to the switching fabric via a data link, and wherein the transmitter transmits data via the data link to the memory for storage therein (refer to Par 0026, 0027 and 0028)"

It would have been obvious to one of ordinary skill in the art to combine Kano with Lay's systems because Lay's teaching of "wherein the transmitting device is contained in a switching fabric, wherein the memory is contained in a line card coupled to the switching fabric via a data link, and wherein the transmitter transmits data via the data link to the memory for storage therein" would improve the system processing speed and off load the host CPU so that instruction decision do not delay packet forwarding.

further comprising the transmitting device, wherein the transmitting device is contained in a switching fabric, wherein the memory is contained in a line card coupled to the switching fabric via a data link, and wherein the transmitter transmits data via the data link to the memory for storage therein.

19. Referring to Claim 27. Kano, Lay and Aimoto disclosed the apparatus of claim 24. Kano further disclosing: a second means for generating a second data quantity value representing a quantity of data stored in the memory device at a second point in time (refer to Col 5, Lines 1-30), wherein the second point in time is prior to the first point in time (refer to Col 5, Lines 1-30); a third means for comparing a data quantity associated with the first data quantity value to the second data quantity value (refer to Col 5, Lines 1-30); wherein the rate control signal is

generated if comparing a data quantity associated with the first data quantity value is not equal to the second data quantity value (refer to Col 5, Lines 1-30);

Although Kano disclosed the invention substantially as claimed, Kano did not explicitly disclosing "comparing the first data quantity value representing a quantity of data stored in the memory with a first predetermined value"

Lay, in analogous art, disclosing that "comparing the first data quantity value representing a quantity of data stored in the memory with a first predetermined value (refer to par 0010)"

It would have been obvious to one of ordinary skill in the art to combine Kano with Lay's systems because Lay's teaching of "comparing the first data quantity value representing a quantity of data stored in the memory with a first predetermined value" would improve the system processing speed and off load the host CPU so that instruction decision do not delay packet forwarding.

20. Referring to Claim 30. Kano discloses a method comprising: a transmitting device transmitting data at a first rate to a memory for storage therein during a first period of time (refer to Col 5, Lines 20-27); generating a first data quantity value representing a quantity of data stored in the memory at a first point in time (determine the size of the buffer not used by generating the count of a data used in buffer, refer to Col 5, Lines 9-11), comparing a data quantity value associated with the first data quantity value to a first predetermined value (refer to Col 5, Lines 20-27); in response to comparing the first data quantity value to the first

predetermined value, the transmitting device transmitting data at a second non-zero rate to the memory for storage therein during a second period of time (refer to Col 5, Lines 25-27); wherein the second period of time is subsequent to the first period of time (refer to Col 5, Lines 25-27), and; wherein the second non-zero rate is less than the first non-zero rate (refer to Col 5, Lines 1-30).

Although Kano disclosed the invention substantially as claimed, Kano did not explicitly disclosing "comparing the first data quantity value representing a quantity of data stored in the memory with a first predetermined value"

Lay, in analogous art, disclosing that "comparing the first data quantity value representing a quantity of data stored in the memory with a first predetermined value (refer to par 0010)"

It would have been obvious to one of ordinary skill in the art to combine Kano with Lay's systems because Lay's teaching of "comparing the first data quantity value representing a quantity of data stored in the memory with a first predetermined value" would improve the system processing speed and off load the host CPU so that instruction decision do not delay packet forwarding.

Although Kano and Lay disclosed the invention substantially as claimed, Kano and Lay did not explicitly disclosing that "modified the first predetermined value"

Aimoto, in analogous art, disclosing that "modified the first predetermined value (refer to Col 10, Lines 35-50)"

It would have been obvious to one of ordinary skill in the art to combine Kano and Lay with Aimoto's system because Aimoto's teaching of " modified the first predetermined value"

would improve Kano and Lay's system by allow efficiently utilizing the buffer and provide better judgment for the congestion of the whole buffer in regard to the total number of cell available.

21. Referring to Claim 31. Kano discloses an apparatus comprising: memory device configured to receive data from a transmitting device for storage therein; a first means for generating and transmitting a rate control signal instructing the transmitting device to stop transmitting data to the memory device at a first non-zero rate and to begin transmitting data to the memory device at a second non-zero rate wherein the second non-zero rate is less than the first non-zero rate (max communication rate is greater than prior rate, refer to Col 5, Lines 5-27), a second means for generating a first data quantity value representing a quantity of data stored in the memory device at a first point in time (determine the size of the buffer not used by generating the count of a data used in buffer, refer to Col 5, Lines 9-11); a third means for comparing a data quantity value associated with the first data quantity value to a first predetermined value (refer to Col 5, Lines 20-27); wherein the first means generates the rate control signal in response to comparing the first data quantity value to the first predetermined value (refer to Col 5, Lines 1-30).

Although Kano disclosed the invention substantially as claimed, Kano did not explicitly disclosing "comparing the first data quantity value representing a quantity of data stored in the memory with a first predetermined value"

Lay, in analogous art, disclosing that "comparing the first data quantity value representing a quantity of data stored in the memory with a first predetermined value (refer to par 0010)"

It would have been obvious to one of ordinary skill in the art to combine Kano with Lay's systems because Lay's teaching of "comparing the first data quantity value representing a quantity of data stored in the memory with a first predetermined value" would improve the system processing speed and off load the host CPU so that instruction decision do not delay packet forwarding.

Although Kano and Lay disclosed the invention substantially as claimed, Kano and Lay did not explicitly disclosing that "modified the first predetermined value"

Aimoto, in analogous art, disclosing that "modified the first predetermined value (refer to Col 10, Lines 35-50)"

It would have been obvious to one of ordinary skill in the art to combine Kano and Lay with Aimoto's system because Aimoto's teaching of " modified the first predetermined value" would improve Kano and Lay's system by allow efficiently utilizing the buffer and provide better judgment for the congestion of the whole buffer in regard to the total number of cell available.

22. Referring to Claim 32. Kano, Lay and Aimoto disclosed the method of claim 30. Kano further disclosing transmitting the rate control signal to the transmitting device to instruct the transmitting device to stop transmitting data at the first non-zero rate and start transmitting data at the second non-zero rate (refer to Col 5, Lines 1-30); wherein the transmitting device

stops transmitting data to the memory device at the first data rate and starts transmitting data to the memory device at the second data rate in response to the transmitting device receiving the rate control signal (refer to Col 5, Lines 1-30).

23. Referring to Claim 34. Kano, Lay and Aimoto disclosed the method of claim 33. Kano further disclosing comparing the first data quantity value to a plurality of predetermined values (refer to Col 5, Lines 1-30), wherein the first predetermined value is one of the plurality of first predetermined values (plurality of thresholds, refer to Col 5, Lines 1-30); wherein the rate control signal is generated in response to comparing the a data quantity value associated with the first data quantity value to the plurality of predetermined values (refer to Col 5, Lines 1-30).

Although Kano disclosed the invention substantially as claimed, Kano did not explicitly disclosing "comparing the first data quantity value representing a quantity of data stored in the memory with a first predetermined value"

Lay, in analogous art, disclosing that "comparing the first data quantity value representing a quantity of data stored in the memory with a first predetermined value (refer to par 0010)"

It would have been obvious to one of ordinary skill in the art to combine Kano with Lay's systems because Lay's teaching of "comparing the first data quantity value representing a quantity of data stored in the memory with a first predetermined value" would improve the system processing speed and off load the host CPU so that instruction decision do not delay packet forwarding.

24. Referring to Claim 35. Kano, Lay and Aimoto disclosed the method of claim 1. Kano further disclosing transmitting the rate control signal to the transmitting device to instruct the transmitting device to stop transmitting data at the first non-zero rate and start transmitting data at the second non-zero rate (refer to Col 5, Lines 1-30); wherein the transmitting device stops transmitting data to the memory device at the first data rate and starts transmitting data to the memory device at the second data rate in response to the transmitting device receiving the rate control signal (refer to Col 5, Lines 1-30).

25. Referring to Claim 37. Kano, Lay and Aimoto disclosed the method of claim 35.

Kano further disclosing comparing the first data quantity value to a plurality of predetermined values (refer to Col 5, Lines 1-30), wherein the first predetermined value is one of the plurality of first predetermined values (plurality of thresholds, refer to Col 5, Lines 1-30); wherein the rate control signal is generated in response to comparing the a data quantity value associated with the first data quantity value to the plurality of predetermined values (refer to Col 5, Lines 1-30).

Although Kano disclosed the invention substantially as claimed, Kano did not explicitly disclosing "comparing the first data quantity value representing a quantity of data stored in the memory with a first predetermined value"

Lay, in analogous art, disclosing that "comparing the first data quantity value representing a quantity of data stored in the memory with a first predetermined value (refer to par 0010)"

It would have been obvious to one of ordinary skill in the art to combine Kano with Lay's systems because Lay's teaching of "comparing the first data quantity value representing a quantity of data stored in the memory with a first predetermined value" would improve the system processing speed and off load the host CPU so that instruction decision do not delay packet forwarding.

26. Referring to Claim 38. Kano, Lay and Aimoto disclosed the method of claim 1. Kano further disclosing transmitting the rate control signal to the transmitting device to instruct the transmitting device to stop transmitting data at the first non-zero rate and start transmitting data at the second non-zero rate (refer to Col 5, Lines 1-30); wherein the transmitting device stops transmitting data to the memory device at the first data rate and starts transmitting data to the memory device at the second data rate in response to the transmitting device receiving the rate control signal (refer to Col 5, Lines 1-30).

27. Referring to Claim 39. Kano, Lay and Aimoto disclosed the method of claim 1.

Although Kano and Lay disclosed the invention substantially as claimed, Kano and Lay did not explicitly disclosing that "subtracting the total data output count from total data input count"

Aimoto, in analogous art, disclosing that "subtracting the total data output count from total data input count value (refer to Cik 13m Kubes 20-35), which is capable to avoid frequent receipt of the rate control signal due to oscillation of the quantity of the data stored within the memory device around the first predetermined value.

It would have been obvious to one of ordinary skill in the art to combine Kano and Lay with Aimoto's system because Aimoto's teaching of " subtracting the total data output count from total data input count" would improve Kano and Lay's system by allow efficiently utilizing the buffer and provide better judgment for the congestion of the whole buffer in regard to the total number of cell available.

28. Referring to Claim 40. Kano, Lay and Aimoto disclosed the apparatus of claim 10.

Although Kano and Lay disclosed the invention substantially as claimed, Kano and Lay did not explicitly disclosing that "subtracting the total data output count from total data input count"

Aimoto, in analogous art, disclosing that "subtracting the total data output count from total data input count value (refer to Cik 13m Kubes 20-35), which is capable to avoid frequent receipt of the rate control signal due to oscillation of the quantity of the data stored within the memory device around the first predetermined value.

It would have been obvious to one of ordinary skill in the art to combine Kano and Lay with Aimoto's system because Aimoto's teaching of " subtracting the total data output count from total data input count" would improve Kano and Lay's system by allow efficiently utilizing the buffer and provide better judgment for the congestion of the whole buffer in regard to the total number of cell available.

29. Referring to Claim 41. Kano, Lay and Aimoto disclosed the apparatus of claim 24.

Although Kano and Lay disclosed the invention substantially as claimed, Kano and Lay did not explicitly disclosing that "subtracting the total data output count from total data input count"

Aimoto, in analogous art, disclosing that "subtracting the total data output count from total data input count value (refer to Cik 13m Kubes 20-35), which is capable to avoid frequent receipt of the rate control signal due to oscillation of the quantity of the data stored within the memory device around the first predetermined value.

It would have been obvious to one of ordinary skill in the art to combine Kano and Lay with Aimoto's system because Aimoto's teaching of " subtracting the total data output count from total data input count" would improve Kano and Lay's system by allow efficiently utilizing the buffer and provide better judgment for the congestion of the whole buffer in regard to the total number of cell available.

30. Referring to Claim 42. Kano, Lay and Aimoto disclosed the apparatus of claim 30.

Although Kano and Lay disclosed the invention substantially as claimed, Kano and Lay did not explicitly disclosing that "subtracting the total data output count from total data input count"

Aimoto, in analogous art, disclosing that "subtracting the total data output count from total data input count value (refer to Cik 13m Kubes 20-35), which is capable to avoid frequent receipt of the rate control signal due to oscillation of the quantity of the data stored within the memory device around the first predetermined value.

It would have been obvious to one of ordinary skill in the art to combine Kano and Lay with Aimoto's system because Aimoto's teaching of " subtracting the total data output count from total data input count" would improve Kano and Lay's system by allow efficiently utilizing the buffer and provide better judgment for the congestion of the whole buffer in regard to the total number of cell available.

31. Referring to Claim 43. Kano, Lay and Aimoto disclosed the apparatus of claim 31.

Although Kano and Lay disclosed the invention substantially as claimed, Kano and Lay did not explicitly disclosing that "subtracting the total data output count from total data input count"

Aimoto, in analogous art, disclosing that "subtracting the total data output count from total data input count value (refer to Cik 13m Kubes 20-35), which is capable to avoid frequent receipt of the rate control signal due to oscillation of the quantity of the data stored within the memory device around the first predetermined value.

It would have been obvious to one of ordinary skill in the art to combine Kano and Lay with Aimoto's system because Aimoto's teaching of " subtracting the total data output count from total data input count" would improve Kano and Lay's system by allow efficiently utilizing the buffer and provide better judgment for the congestion of the whole buffer in regard to the total number of cell available.

Conclusion

Examiner's Notes: Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner. In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

A shortened statutory period for reply to this Office action is set to expire THREE MONTHS from the mailing date of this action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Karen C. Tang whose telephone number is (571)272-3116. The examiner can normally be reached on M-F 7 - 3.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Follansbee can be reached on (571)272-3964. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Karen C Tang/
Examiner, Art Unit 2451

/Larry D Donaghue/
Primary Examiner, Art Unit 2454